LISTING OF CLAIMS

Claims 1-2. (Canceled).

3. (Currently Amended) A circuit, comprising:

a memory array comprising a plurality of memory cells, the plurality of memory cells arranged in a plurality of groups, each memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry selectively coupled, one group at time, to source terminals of the n-channel transistors in the selected group, for providing to those source terminals a low voltage reference level during a normal mode of operation and transitioning those source terminals to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation, the power control circuitry comprising:

a counter;

a plurality of decoders, one decoder per group, each decoder coupled to receive a count value output from the counter and decode that count value to selectively transition that decoder's connected n-channel source terminal from the low voltage reference level to the high voltage reference level and back to the low voltage reference level.

4. (Canceled).

5. (Original) The circuit of claim 3 wherein the source terminal of the other n-channel transistor in each memory cell is always coupled to the low voltage reference.

Claims 6-8. (Canceled).

9. (Currently Amended) A method for clearing a volatile memory cell, wherein the volatile memory cell is part of a memory array including a plurality of like volatile memory cells, the volatile memory cells arranged in a plurality of groups, comprising:

counting to produce a count value;

decoding the count value in association with each group; and

wherein, for a given group, if the decoding of the count value is true:

transitioning a low voltage reference terminal for the ~~[a]~~ memory cells for that given group ~~cell~~ from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation; and

transitioning the low voltage reference terminal for the memory cells for that given group from the high reference voltage back to the low reference voltage.

10. (Original) The method of claim 9 wherein the memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell.

11. (Original) The method of claim 10 further comprising holding a source terminal of another n-channel transistor in the latch portion of the memory cell at the low reference voltage.

12. (Canceled).

13. (Currently Amended) A circuit, comprising:

a memory array including a plurality of volatile memory cells, the memory cells arranged in a plurality of groups, wherein each ~~[a]~~ volatile memory cell has ~~having~~ a low voltage reference terminal; and

power control circuitry coupled to the volatile memory cells ~~cell~~ that selectively transitions, one group at a time, the low voltage reference terminal of cells in the selected group, from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation and then back ~~transitions the low voltage reference terminal~~ from the high reference voltage back to the low reference voltage, the power control circuitry comprising:

a counter;

a plurality of decoders, one decoder per group, each decoder coupled to receive a count value output from the counter and decode that count value to cause selective transition at the low voltage reference terminal for cells in the selected group.

14. (Original) The circuit of claim 13 wherein the volatile memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell.

15. (Original) The circuit of claim 14 wherein a source terminal of another n-channel transistor in the latch is always coupled to the low reference voltage.

16. (Canceled).

17. (Currently Amended) A method for clearing a volatile memory cell, wherein the volatile memory cell is part of a memory array including a plurality of like volatile memory cells, comprising:

simultaneously transitioning a high voltage reference terminal for all ~~[a]~~ volatile memory cells in the array ~~cell~~ from a high reference voltage associated with a normal mode of operation to a low reference voltage in a data corruption mode of operation, and then returning the high voltage reference terminal back to the high reference voltage; and

simultaneously transitioning a low voltage reference terminal for all ~~the~~ volatile memory cells in the array ~~cell~~ from the low reference voltage associated with the normal mode of operation to the high reference voltage in a data corruption mode of operation, and then returning the low voltage reference terminal back to the low reference voltage.

18. (Original) The method of claim 17 wherein the memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell and the high voltage reference terminal comprises a source terminal of at least one p-channel transistor in the latch portion of the memory cell.

19. (Original) The method of claim 18 further comprising holding a source terminal of another n-channel transistor in the latch portion of the memory cell at the low reference voltage.

20. (Canceled).

21. (Original) The method of claim 17 wherein the steps of transitioning voltage on the low and high voltage reference terminals are performed in an interleaved manner.

22. (Currently Amended) A circuit, comprising:

a memory array including a plurality of volatile memory cells, wherein each ~~[a]~~ volatile memory cell has ~~having~~ a low voltage reference terminal and a high voltage reference terminal; and

power control circuitry coupled to the volatile memory cells, the power control circuitry including voltage driver circuitry operable to simultaneously transition ~~cell that transitions~~:

a) the high voltage reference terminal of all cells in the array from a high reference voltage associated with a normal mode of operation to a low reference voltage in a data corruption mode of operation and back to the high reference voltage; and

b) the low voltage reference terminal of all cells in the array from a low reference voltage associated with a normal mode of operation to a high reference voltage in a data corruption mode of operation and back to the low reference voltage.

23. (Original) The circuit of claim 22 wherein the volatile memory cell comprises a 6T memory cell and the low voltage reference terminal comprises a source terminal of one n-channel transistor in a latch portion of the memory cell and the high voltage reference terminal comprises a source terminal of at least one p-channel transistor in the latch portion of the memory cell.

24. (Original) The circuit of claim 23 wherein a source terminal of another n-channel transistor in the latch is always coupled to the low reference voltage.

25. (Canceled).

26. (Original) The circuit of claim 22 wherein the power control circuitry transitions voltage on the low and high voltage reference terminals in an interleaved manner.

27. (Currently Amended) A circuit, comprising:

a memory array comprising a plurality of memory cells, each memory cell having first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration; and

power control circuitry:

a) coupled to a source terminal of at least one of the p-channel transistors in each of the memory cells within the memory array for providing to those source terminals a high voltage reference level during a normal mode of operation and simultaneously driving ~~transitioning~~ those source terminals for all cells in the array to a low voltage reference level and back to the high voltage reference level during a data corruption mode of operation; and

b) coupled to a source terminal of one of the n-channel transistors in each of the memory cells within the memory array for providing to those source terminal the low voltage reference level during the normal mode of operation and simultaneously driving ~~transitioning~~ those source terminals for all cells in the array to the high voltage reference level and back to the low voltage reference level during a data corruption mode of operation.

28. (Original) The circuit of claim 27 wherein the source terminal of the other n-channel transistor in each of the memory cells within the memory array is always coupled to the low voltage reference.

29. (Currently Amended) The circuit of claim 27 wherein the power control circuitry simultaneously transitions voltage across the array on the source terminal of the at least one p-channel transistor and simultaneously transitions voltage across the array on the source terminal of the n-channel transistor in each of the memory cells within the memory array in an interleaved manner.